REMARKS

Claims 1-6 have been amended, without prejudice or surrender of any subject matter, to correct informalities and to more clearly recite the representative embodiments of the invention. Claims 7-9 have been added to point out further embodiments of the invention. Accordingly, claims 1-9 are presented for examination.

Waiver of 37 CFR 1.121(a), (b), (c), & (d)

This amendment and response paper is submitted in a format as set forth in the January 31, 2003, pre-OG notice of change in examination policy by the Deputy Commissioner for Patents. The notice indicates a waiver of the provisions in 37 1.121(a), (b), (c), & (d) for amendments to claims, specification and drawings.

The specification

The specification has been amended to correct informalities and to render the specification consistent with the drawings. No new matter has been introduced by this amendment.

The Drawings

Figures 4b, 5a, and 5b have been amended. Submitted herewith are substitute Figures 4b, 5a, and 5b, including all the changes made. In Figure 4b, designation numbers 152 and 154 have been added to indicate respective states of data from the Q output of FF1 (as described in pages 10 and 11 of Applicant's specification). In Figure 5a, the multiplexer designation number, 120, has been changed to 122 so as to match the illustration in Figure 3. In Figure 5b, the designation 154' has been added to render Figures 4b and 5b consistent with each other and with the specification. No new matter has been introduced by this amendment. Approval of the amendment to the drawings is hereby requested.

The claims

Claims 1-6 have been rejected under 35 U.S.C. as being anticipated by U.S. Patent 5,689,517 to Ruparel. However, Ruparel neither teaches nor suggests each and every element of

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the claimed embodiments of the invention as recited in claims 1-6, nor does Ruparel enable the practice of the claimed embodiments. Therefore, the claims are not anticipated by Ruparel.

In general, claims 1-6 recite representative embodiments of a scheme directed to deterministic testing of edge-triggered logic that, among others, employs a latch, or latch element, in the scan path... between the two devices (e.g., edge-triggered devices as in claim 1 or clock domains with edge-triggered devices as in claim 5. By contrast, Ruparel does not teach or suggest a scheme for deterministic testing of edge-triggered logic nor does it teach or suggest a latch in the scan data path (...between the two devices).

Nonetheless, in support of the claim rejection, the Examiner points to Ruparel's Figures 1a, 1b, 2b and 6a. However, it is easy to visualize the difference between the claimed invention as recited in claims 1-6 and the configurations shown in Ruparel's Figures.

More specifically, consider for example the embodiment of a circuit for deterministic testing of edge-triggered logic, as recited in claim 1. This circuit includes at least first and second edge-triggered devices, each being clocked by a respective clock signal. Namely, each device receives and corresponding clock. A selectable circuit path is included in the circuit for forming a scan data path that includes the first and second edge-triggered devices. The circuit further includes a latch in the scan data path. The latch has an input coupled to an output of the first edge-triggered device and an output coupled to an input of the second edge-triggered device. Namely, the latch is in the path between the two devices. The latch is clocked by a test-clock signal to temporarily hold data previously held by the first edge-triggered device while the first and second edge-triggered devices change state.

By comparison, in Figure 1a, Ruparel shows two latches (11, 12) forming a shift register function. Clearly, Figure 1a and the accompanying description in col. 1 does not show or suggest a latch in the scan data path (...between the two devices). And, even though the shift registers (10a, 10b & 10c) are cascaded in Figure 1b, there is no latch in the respective scan paths (between the corresponding pairs of shift registers). The Examiner appears to suggest that the cascaded shift register produce the circuit of claim 1 in that it shows latches and a scan path.

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However, even with a scan path through the shift registers, Ruparel's circuit as shown in Figure 1b is not configured to perform deterministic testing of edge-triggered logic. Indeed, the latches in Ruparel, 11a, 11b, and 11c, receive the same clock rather than respective clocks. Namely, these latches coexist in the same time domain unlike the two devices in the circuit of claim 1.

Moreover, considering for example claim 2, the circuit in Ruparel's Figure 1b does not include multiplexers for selectively forming the scan path. The multiplexer shown in Figure 2a and those shown in Figure 2b form a scan path but not in a circuit having a latch in the scan path between the two device (unlike the circuit of claims 1 –4 and, by analogy, claim 5). Notably, as alluded to before, Ruparel does not address, nor does it suggest or show how to address, deterministic testing of logic with devices in separate time domains, as provided in claims 1-4, 5, and 6.

Indeed, Ruparel discloses a scheme for observing test data in scannable-D-flip-flops independent of the system clock and without affecting data in the non-scannable flip-flops (See, e.g., abstract and col. 7 lines 9-16). Stated another way, Ruparel's Figures (and accompanying descriptions) show individual elements of a circuit configured for one instance of scan testing. However, Ruparel's Figures and descriptions do not go as far as showing or suggesting even one combination that includes all the elements of the claimed embodiments of the invention as recited in claims 1-6.

In view of the abovementioned Figures, and considering Ruparel's disclosure as a whole, Ruparel's does not enable the circuit or method as recited, respectively, in claims 1-6. Clearly, Ruparel's teaching is non-enabling as to a deterministic test of edge-triggered logic.

Accordingly, claims 1-6 are allowable over Ruparel. Reconsideration and withdrawal of the claim rejections are hereby solicited in view of the foregoing.

New claims

Claims 7-9, have been added to point out further embodiments and variations of the aforementioned scheme. The foregoing applies to the new claims with equal force and effect. Accordingly, claims 7-9 are also allowable.

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CONCLUSION

The Application is believed to be in condition for allowance, and a Notice of Allowance is hereby requested.

If the Examiner believes that a conference would be helpful in expediting the prosecution of this application, the Examiner is kindly invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

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